APPLICATION NO. 10634446

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CLMPTO

1. A method of forming an integrated semiconductor structure comprising:

providing an SOI substrate comprising a top semiconductor layer of a first crystallographic orientation and a bottom semiconductor layer of a second crystallographic orientation separated by an insulating layer, said first crystallographic orientation is different from said second crystallographic orientation;

forming at least one opening in the SOI substrate that exposes a surface of the bottom semiconductor layer;

growing a semiconductor material on said exposed surface of the bottom semiconductor layer, said semiconductor material having a crystallographic orientation that is the same as the second crystallographic orientation;

forming a buried insulating region in said semiconductor material by ion implantation and annealing, said buried insulating region separates the semiconductor material from said bottom semiconductor layer; and

planarizing the implanted semiconductor material to provide a structure in which the semiconductor material having the second crystallographic orientation is substantially coplanar and of substantially the same thickness as that of the top semiconductor layer.

2. The method of Claim 1 wherein the providing the SOI substrate comprises bonding two wafers together, wherein at least one wafer includes the top semiconductor layer and the other wafer includes the bottom semiconductor layer.

3. The method of Claim 1 wherein said SOI substrate further includes a surface dielectric formed thereon.

4. The method of Claim 1 wherein said forming at least one opening comprising forming a patterned mask on the SOI substrate and etching.

5. The method of Claim 1 further comprising forming a spacer on exposed sidewalls of the least one opening prior to said growing the semiconductor material.

6. The method of Claim 5 wherein said spacer is formed by deposition and etching.

7. The method of Claim 1 wherein the growing the semiconductor material comprises a selective epitaxial growth process.

8. The method of Claim 1 wherein the ion implantation comprises implanting oxygen or nitrogen ions within the semiconductor material.

9. The method of Claim 1 wherein the ion implantation comprises a base ion implant step.

10. The method of Claim 9 further comprising a second ion implantation step after the base ion implant step.

11. The method of Claim 1 wherein the annealing is performed at a temperature of from about 700° to about 1400°C in an oxidizing ambient.

12. The method of Claim 1 wherein the oxidizing ambient includes an oxygen-containing gas that may optionally be diluted with an inert gas.

13. The method of Claim 1 wherein said planarizing includes at least one etching step in which oxide is selectively removed.

14. The method of Claim 1 further comprising forming at least one pFET and a least one nFET on said structure.

15. The method of Claim 14 wherein the at least one pFET is located on a (110) crystallographic surface, while the at least one nFET is located on a (100) crystallographic surface.

16. The method of Claim 1 wherein the top semiconductor layer has a (110) surface orientation and the semiconductor material has a (100) surface orientation.

17. The method of Claim 16 further comprising forming at least one pFET on the (110) surface and at least one nFET the (100) surface.

CLAIMS 18-25 (CANCELLED)